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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Chien-Hao Chen

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10/31/2005

THOMAS, KAYDEN, HOSTEMEYER & RISLEY LLP
100 GALLERIA PARKWAY
SUITE 1750
ATLANTA, GA 30339

EXAMINER

CHEN, JACK S J

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/810,795	Applicant(s) CHEN ET AL.	
	Examiner Jack Chen	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-14,16-25 and 40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-14,16-25 and 40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>8/2/05</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

In response to the communication filed on August 9, 2005, claims 1, 3-14, 16-25 and 40 are active in this application.

Information Disclosure Statement

The information disclosure statement filed August 2, 2005 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5-6, 10-12, 14, 18-19, 23-24 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Saitoh, U.S. Pub. Number: 2003/0040158 A1.

Re claims 1 and 14, Saitoh discloses a method for forming semiconductor device, which comprises providing a semiconductor substrate 1 comprising gate structures 13/6 and offset spacers 7a/7b overlying respective PMOS and NMOS device regions (fig. 3A); forming source/drain regions 10s/11s (fig. 3a); forming silicides 12a/12b/12d/12e over the source/drain regions and over 12c/12f an upper portion of the respective gate structure (fig. 3A); forming a first dielectric layer 14 comprising a stress type selected from the group consisting of tensile stress and compressive stress (i.e., tensile stress) over the respective PMOS and NMOS device regions (fig. 3A); forming a buffer oxide layer 19 (BPSG is oxide) overlying the first dielectric layer (fig. 2); removing a portion of the first dielectric layer overlying one of the PMOS and NMOS device regions (fig. 3B); forming a second dielectric layer 16 comprising a stress type opposite (i.e., compressive stress) from the first dielectric layer stress type over the respective PMOS and NMOS device regions (fig. 3C); and removing the second dielectric layer overlying one of the PMOS and NMOS device regions to form a compressive stress dielectric layer 16 over the PMOS device region and a tensile stress dielectric layer 14 over the NMOS device region (fig. 2), see figs. 1A-5 and pages 1-8 for more details.

Re claim 40, Saitoh discloses a method for forming semiconductor device, which comprises providing a semiconductor substrate 1 comprising a first gate structure 13 overlying a PMOS device region and a second gate structure 6 overlying a NMOS device region (fig. 2); forming a first layer 14 with first stress over the NMOS region; forming a buffer oxide layer 19 (BPSG is oxide) overlying the first dielectric layer (fig. 2) and forming a second layer 16 with second stress over the PMOS region such that an interface 20 is formed between the first layer

and the second layer (fig. 2); wherein the second stress is different from the first stress, see figs. 1A-5 and pages 1-8 for more details.

Re claims 5 and 18, wherein the first and second dielectric layers comprises a material selected from the group consisting of silicon nitride and silicon oxynitride (i.e. silicon nitride), see paragraph 102-103.

Re claims 6 and 19, wherein the first and second dielectric layers are formed by a CVD deposition process selected from the group consisting of LPCVD, ALCVD, and PECVD, see paragraph 102-103.

Re claim 10, wherein the silicide comprises a metal silicide, see paragraph 100.

Re claims 11 and 23, wherein the metal silicide is selected from the group consisting of cobalt silicide and titanium silicide, see paragraph 100.

Re claims 12 and 24, wherein the first and second dielectrics layers are formed without a subsequent ion implantation process to relieve a stress level (in this case, no subsequent ion implantation process to relieve a stress level).

3. Claims 1, 3-14, 16-25 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Hachimine et al., U.S. Pub. No. 2003/0181005 A1.

Re claims 1 and 14, Hachimine et al. disclose a method for forming semiconductor device, which comprises providing a semiconductor substrate 1 comprising gate structures 6 and offset spacers 9 overlying respective PMOS and NMOS device regions (fig. 6); forming source/drain regions 7/10/8/11 (fig. 6); forming silicides 12 over the source/drain regions and over an upper portion of the respective gate structure (fig. 9); forming a first dielectric layer 14a comprising a stress type selected from the group consisting of tensile stress and compressive

stress (i.e., tensile stress) over the respective PMOS and NMOS device regions (fig. 11); forming a buffer oxide layer 15 overlying the first dielectric layer (fig. 12); removing a portion of the first dielectric layer overlying one of the PMOS and NMOS device regions (fig. 14); forming a second dielectric layer 14b comprising a stress type opposite (i.e., compressive stress) from the first dielectric layer stress type over the respective PMOS and NMOS device regions (fig. 15); and removing the second dielectric layer overlying one of the PMOS and NMOS device regions to form a compressive stress dielectric layer 14b over the PMOS device region and a tensile stress dielectric layer 14a over the NMOS device region (fig. 1), see figs. 1-44 and pages 1-21 for more details.

Re claim 40, Hachimine et al. disclose a method for forming semiconductor device, which comprises providing a semiconductor substrate 1 comprising a first gate structure 6 overlying a PMOS device region and a second gate structure 6 overlying a NMOS device region (fig. 6); forming a first layer 14a with first stress over the NMOS region (fig. 11); forming a buffer oxide layer 15 overlying the first dielectric layer (fig. 12) and forming a second layer 14b with second stress over the PMOS region such that an interface is formed between the first layer and the second layer (fig. 15); wherein the second stress is different from the first stress, see figs. 1-44 and pages 1-21 for more details.

Re claims 3 and 16, wherein the buffer oxide layer 15 comprises a silicon oxide layer (paragraph 0196).

Re claims 4 and 17, wherein the buffer oxide layer is from about 10 to about 1000 angstroms (i.e., 50nm) in thickness (paragraph 0196).

Art Unit: 2813

Re claims 5 and 18, wherein the first and second dielectric layers comprises a material selected from the group consisting of silicon nitride and silicon oxynitride (i.e. silicon nitride), see paragraph 194 and 202.

Re claims 6 and 19, wherein the first and second dielectric layers are formed by a CVD deposition process selected from the group consisting of LPCVD, ALCVD, and PECVD, see paragraph 194 and 202.

Re claims 7 and 20, wherein the first and second dielectric layers are formed by precursors comprising silane (paragraph 232).

Re claims 8 and 21, wherein the first and second dielectric layers are 10 to about 1000 angstroms (i.e., about 100nm) in thickness (paragraph 194 and 202).

Re claims 9 and 22, wherein the compressive stress dielectric layer and the tensile stress dielectric layer comprise a stress level up to about 2 Gpa (paragraph 175).

Re claim 10, wherein the silicide comprises a metal silicide, see paragraph 191.

Re claims 11 and 23, wherein the metal silicide is selected from the group consisting of cobalt silicide and titanium silicide, see paragraph 191.

Re claims 12 and 24, wherein the first and second dielectrics layers are formed without a subsequent ion implantation process to relieve a stress level (in this case, no subsequent ion implantation process to relieve a stress level in the first and second dielectric layer).

Re claims 13 and 25, wherein the first and second dielectric layers form a contact etching stop layer in a subsequent damascene formation process (fig. 1 and paragraph 173).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2813

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jack Chen
Primary Examiner
Art Unit 2813

October 29, 2005